

9. Digital one-shots are implemented with a counter loaded with a delay value when the trigger input is detected and counts down to zero. During the countdown time, the output pulse is held HIGH.
10. With strategic placement of the hardware description statements, HDL one-shots can be made edge- or level-triggered and retriggerable or nonretriggerable. They produce an output pulse that responds synchronously or asynchronously to the trigger.

PART 2 IMPORTANT TERMS

parallel in/parallel out	circulating shift register	sequential logic system
serial in/serial out	ring counter	LPM_SHIFTREG
parallel in/serial out	Johnson counter (twisted	concatenation
serial in/parallel out	ring counter)	digital one-shot

PROBLEMS

PART 1

SECTION 7-1

- B** 7-1* Add another flip-flop, *E*, to the counter of Figure 7-1. The clock signal is an 8-MHz square wave.
- (a) What will be the frequency at the *E* output? What will be the duty cycle of this signal?
 - (b) Repeat (a) if the clock signal has a 20% duty cycle.
 - (c) What will be the frequency at the *C* output?
 - (d) What is the MOD number of this counter?
- B** 7-2. Draw a binary counter that will convert a 64-kHz pulse signal into a 1-kHz square wave.
- B** 7-3* Assume that a five-bit binary counter starts in the 00000 state. What will be the count after 144 input pulses?
- B** 7-4. A 10-bit ripple counter has a 256-kHz clock signal applied.
- (a) What is the MOD number of this counter?
 - (b) What will be the frequency at the MSB output?
 - (c) What will be the duty cycle of the MSB signal?
 - (d) Assume that the counter starts at zero. What will be the count in hexadecimal after 1000 input pulses?

SECTION 7-2

- 7-5* A four-bit ripple counter is driven by a 20-MHz clock signal. Draw the waveforms at the output of each FF if each FF has $t_{pd} = 20$ ns. Determine which counter states, if any, will not occur because of the propagation delays.
- 7-6. (a) What is the maximum clock frequency that can be used with the counter of Problem 7-5?
- (b) What would f_{max} be if the counter were expanded to six bits?

* Answers to problems marked with an asterisk can be found in the back of the text.

SECTIONS 7-3 AND 7-4

- B** 7-7* (a) Draw the circuit diagram for a MOD-32 synchronous counter.
 (b) Determine $f_{\max}$ for this counter if each FF has $t_{pd} = 20$ ns and each gate has $t_{pd} = 10$ ns.
- B** 7-8. (a) Draw the circuit diagram for a MOD-64 synchronous counter.
 (b) Determine $f_{\max}$ for this counter if each FF has $t_{pd} = 20$ ns and each gate has $t_{pd} = 10$ ns.
- B, N** 7-9. The decade counter in Figure 7-8(b) has a 1-kHz clock applied.
 (a) Draw the waveforms for each FF output, showing any glitches that may occur.
 (b) Determine the frequency of the signal at the D output.
 (c) If the counter is originally at state 1000, what state will the counter be at after 14 clock pulses are applied?
 (d) If the counter is originally at state 0101, what state will the counter be at after 20 clock pulses are applied?
- B** 7-10. Repeat Problem 7-9 for the counter of Figure 7-8(a) with a 70-kHz clock.
- 7-11* Change the inputs to the NAND gate of Figure 7-9 so that the counter divides the input frequency by 50.
- D** 7-12. Draw a synchronous counter that will output a 10-kHz signal when a 1-MHz clock is applied.

SECTIONS 7-5 AND 7-6

- B** 7-13* Draw a synchronous, MOD-32, down counter.
- B** 7-14. Draw a synchronous, MOD-16, up/down counter. The count direction is controlled by dir ($dir = 0$ to count up).
- C, T** 7-15* Determine the count sequence of the up/down counter in Figure 7-11 if the INVERTER output were stuck HIGH. Assume the counter starts at 000.
- 7-16. Complete the timing diagram in Figure 7-102 for the presettable counter in Figure 7-12. Note that the initial condition for the counter is given in the timing diagram.

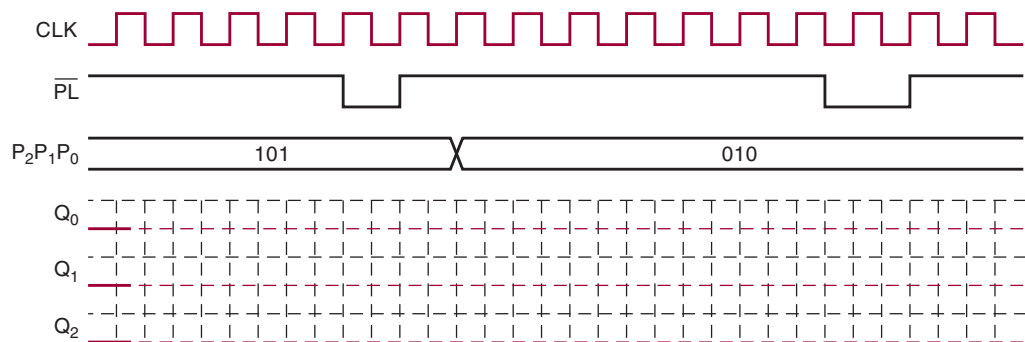


FIGURE 7-102 Problem 7-16 timing diagram.

SECTION 7-7

7-17* Complete the timing diagram in Figure 7-103 for a 74ALS161 with the indicated input waveforms applied. Assume the initial state is 0000.

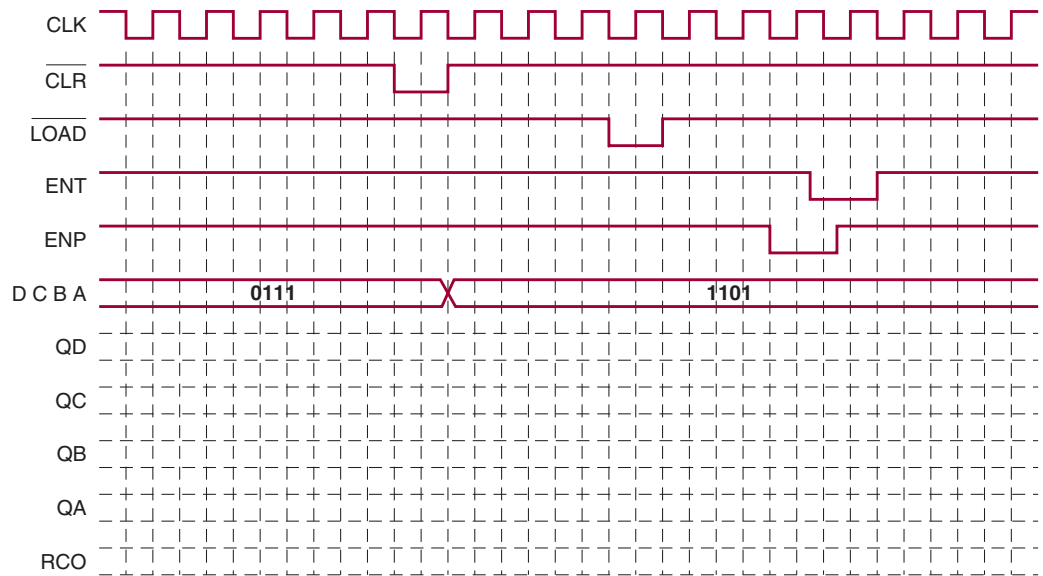


FIGURE 7-103 Problem 7-17 timing diagram.

7-18. Complete the timing diagram in Figure 7-104 for a 74ALS162 with the indicated input waveforms applied. Assume the initial state is 0000.

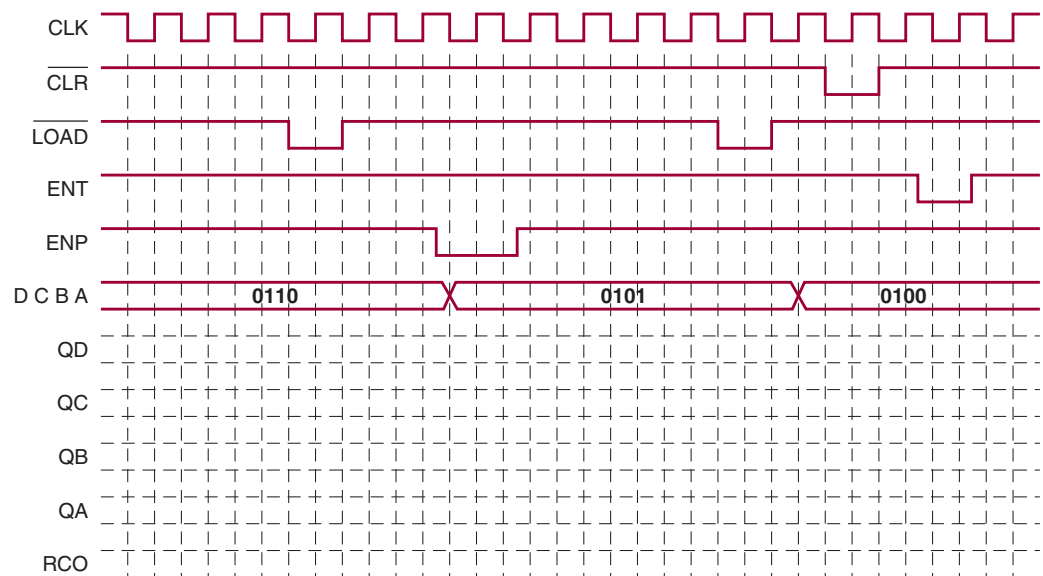


FIGURE 7-104 Problem 7-18 timing diagram.

7-19* Complete the timing diagram in Figure 7-105 for a 74ALS190 with the indicated input waveforms applied. The *DCBA* input is 0101.

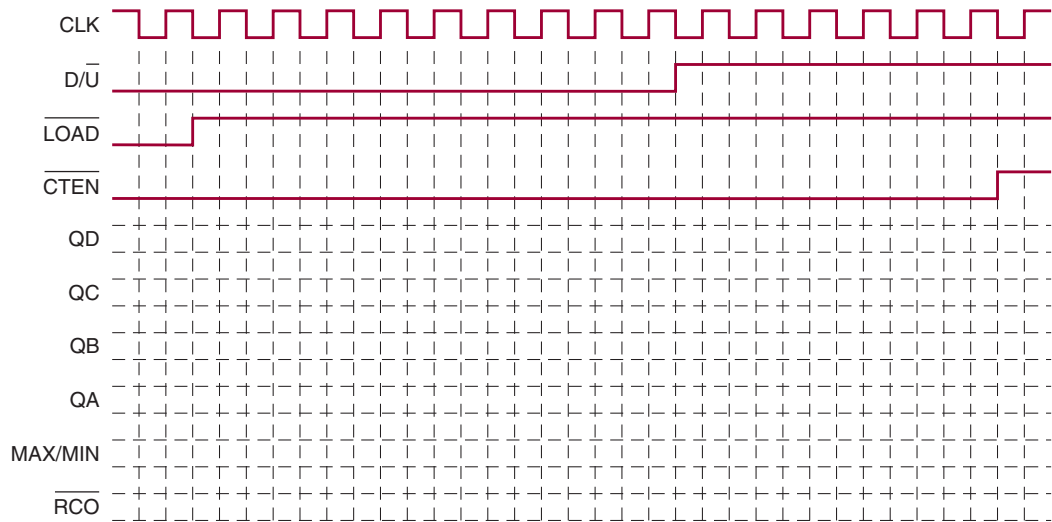


FIGURE 7-105 Problems 7-19 and 7-20 timing diagram.

7-20. Repeat Problem 7-19 for a 74ALS191 and a *DCBA* input of 1100.

B 7-21* Refer to the IC counter circuit in Figure 7-106(a):

- Draw the state transition diagram for the counter's *QD QC QB QA* outputs.
- Determine the counter's modulus.

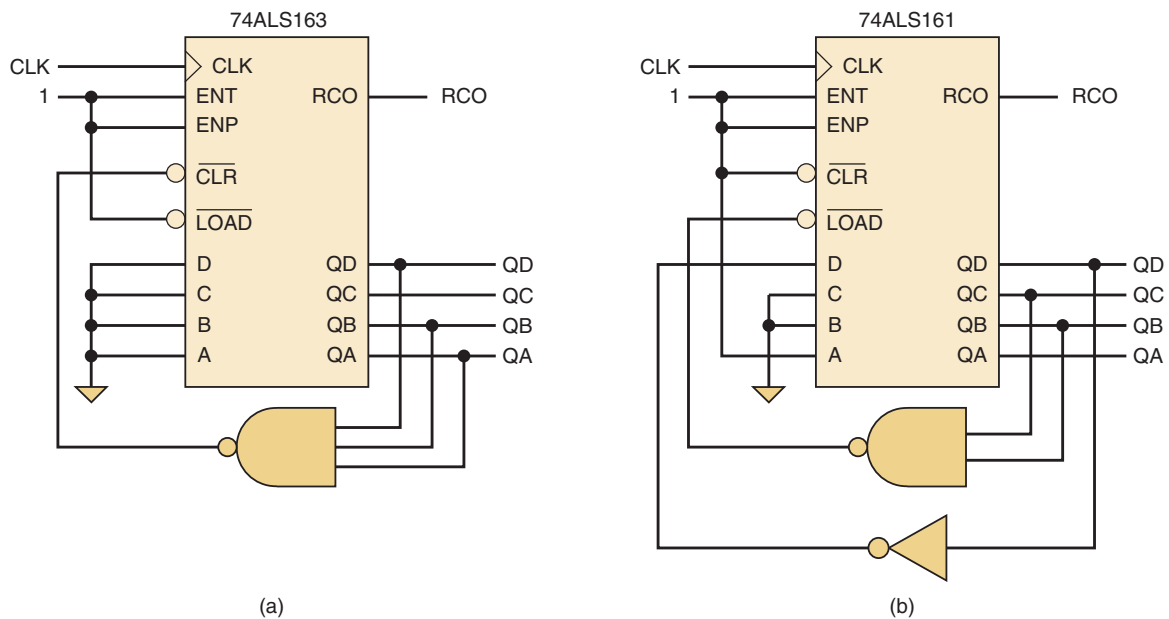


FIGURE 7-106 Problems 7-21 and 7-22

- (c) What is the relationship of the output frequency of the MSB to the input CLK frequency?
- (d) What is the duty cycle of the MSB output waveform?
- B** 7-22. Repeat Problem 7-21 for the IC counter circuit in Figure 7-106(b).
- B** 7-23* Refer to the IC counter circuit in Figure 7-107(a).
- (a) Draw the timing diagram for outputs QD QC QB QA .
- (b) What is the counter's modulus?
- (c) What is the count sequence? Does it count up or down?
- (d) Can we produce the same modulus with a 74HC190? Can we produce the same count sequence with a 74HC190?

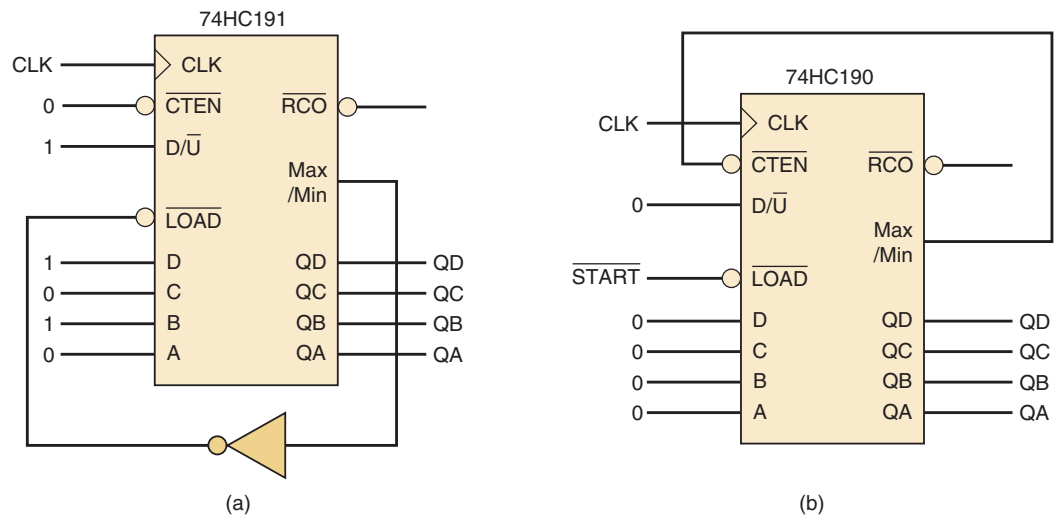


FIGURE 7-107 Problems 7-23 and 7-24.

- 7-24. Refer to the IC counter circuit in Figure 7-107(b):
- (a) Describe the counter's output on QD QC QB QA if $\overline{START}$ is LOW.
- (b) Describe the counter's output on QD QC QB QA if $\overline{START}$ is momentarily pulsed LOW and then returns to a HIGH.
- (c) What is the counter's modulus? Is this a recycling counter?
- D** 7-25* Draw a schematic to create a recycling, MOD-6 counter that uses:
- (a) the clear control on a 74ALS160
- (b) the clear control on a 74ALS162
- D** 7-26. Draw a schematic to create a recycling, MOD-6 counter that produces the count sequence:
- (a) 1, 2, 3, 4, 5, 6, and repeats with a 74ALS162
- (b) 5, 4, 3, 2, 1, 0, and repeats with a 74ALS190
- (c) 6, 5, 4, 3, 2, 1, and repeats with a 74ALS190
- D** 7-27* Design a MOD-100, binary counter using either two 74HC161 or two 74HC163 chips and any necessary gates. The IC counter chips are to be synchronously cascaded together to produce the binary count sequence for 0 to 99. The MOD-100 is to have two control inputs,

an active-LOW count enable ($\overline{EN}$) and an active-LOW, asynchronous clear ($\overline{CLR}$). Label the counter outputs Q_0 , Q_1 , Q_2 , and so on, with Q_0 = LSB. Which output is the MSB?

- D** 7-28. Design a MOD-100, BCD counter using either two 74HC160 or two 74HC162 chips and any necessary gates. The IC counter chips are to be synchronously cascaded together to produce the BCD count sequence for 0 to 99. The MOD-100 is to have two control inputs, an active-HIGH count enable (EN) and an active-HIGH, synchronous load (LD). Label the counter outputs Q_0 , Q_1 , Q_2 , and so on, with Q_0 = LSB. Which set of outputs represents the 10s digit?
- B** 7-29* With a 6-MHz clock input to a 74ALS163 that has all four control inputs HIGH, determine the output frequency and duty cycle for each of the *five* outputs (including RCO).
- B** 7-30. With a 6-MHz clock input to a 74ALS162 that has all four control inputs HIGH, determine the output frequency and duty cycle for each of the following outputs: QA , QC , QD , RCO . What is unusual about the waveform pattern that would be produced by the QB output? This pattern characteristic results in an undefined duty cycle.
- B** 7-31* The frequency of f_{in} is 6 MHz in Figure 7-108. The two IC counter chips have been cascaded asynchronously so that the output frequency produced by counter U1 is the input frequency for counter U2. Determine the output frequency for f_{out1} and f_{out2} .

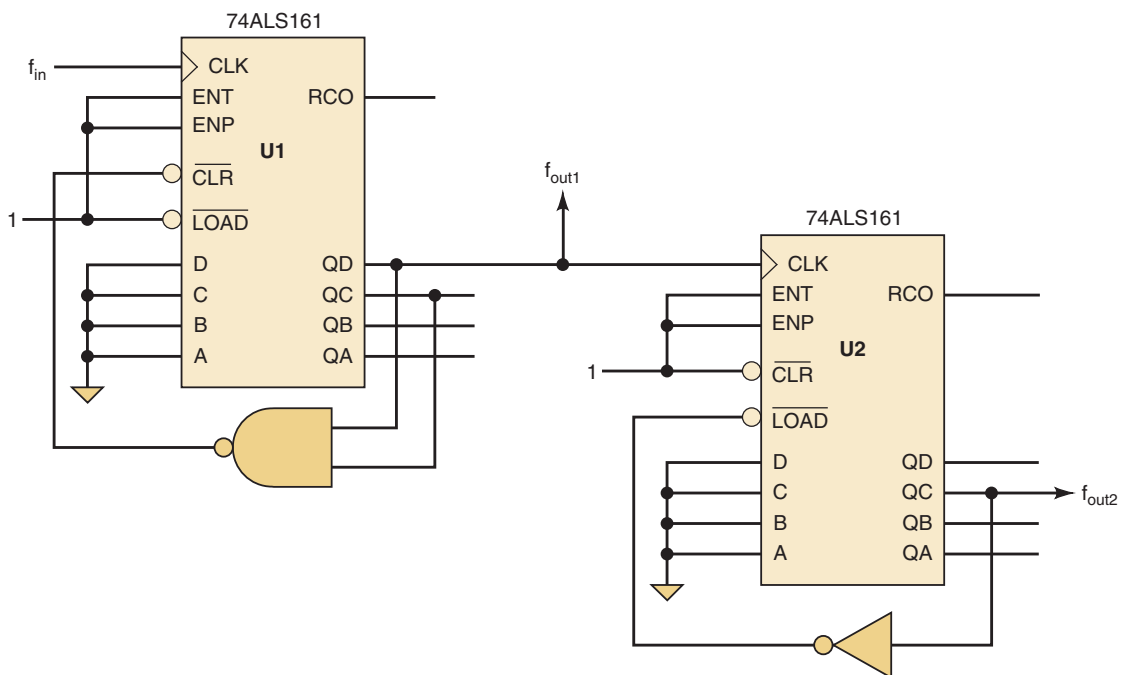


FIGURE 7-108 Problem 7-31.

- B** 7-32. The frequency of f_{in} is 1.5 MHz in Figure 7-109. The two IC counter chips have been cascaded asynchronously so that the output frequency produced by counter U1 is the input frequency for counter U2. Determine the output frequency for f_{out1} and f_{out2} .

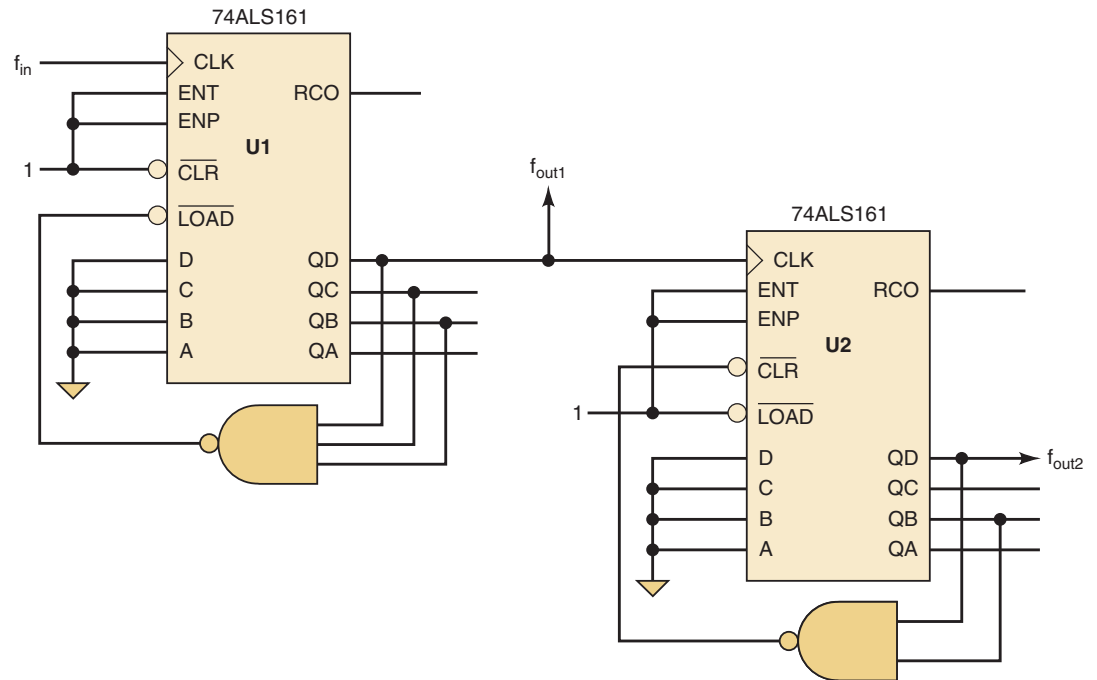


FIGURE 7-109 Problem 7-32.

- D** 7-33* Design a frequency divider circuit that will produce the following three output signal frequencies: 1.5 MHz, 150 kHz, and 100 kHz. Use 74HC162 and 74HC163 counter chips and any necessary gates. The input frequency is 12 MHz.
- D** 7-34. Design a frequency divider circuit that will produce the following three output signal frequencies: 1 MHz, 800 kHz, and 100 kHz. Use 74HC160 and 74HC161 counter chips and any necessary gates. The input frequency is 12 MHz.

SECTION 7-8

- B** 7-35* Draw the gates necessary to decode all of the states of a MOD-16 counter using active-LOW outputs.
- B** 7-36. Draw the AND gates necessary to decode the 10 states of the BCD counter of Figure 7-8(b).

SECTION 7-9

- C** 7-37* Analyze the synchronous counter in Figure 7-110(a). Draw its timing diagram and determine the counter's modulus.
- C** 7-38. Repeat Problem 7-37 for Figure 7-110(b).
- C** 7-39* Analyze the synchronous counter in Figure 7-111(a). Draw its timing diagram and determine the counter's modulus.
- C** 7-40. Repeat Problem 7-39 for Figure 7-111(b).

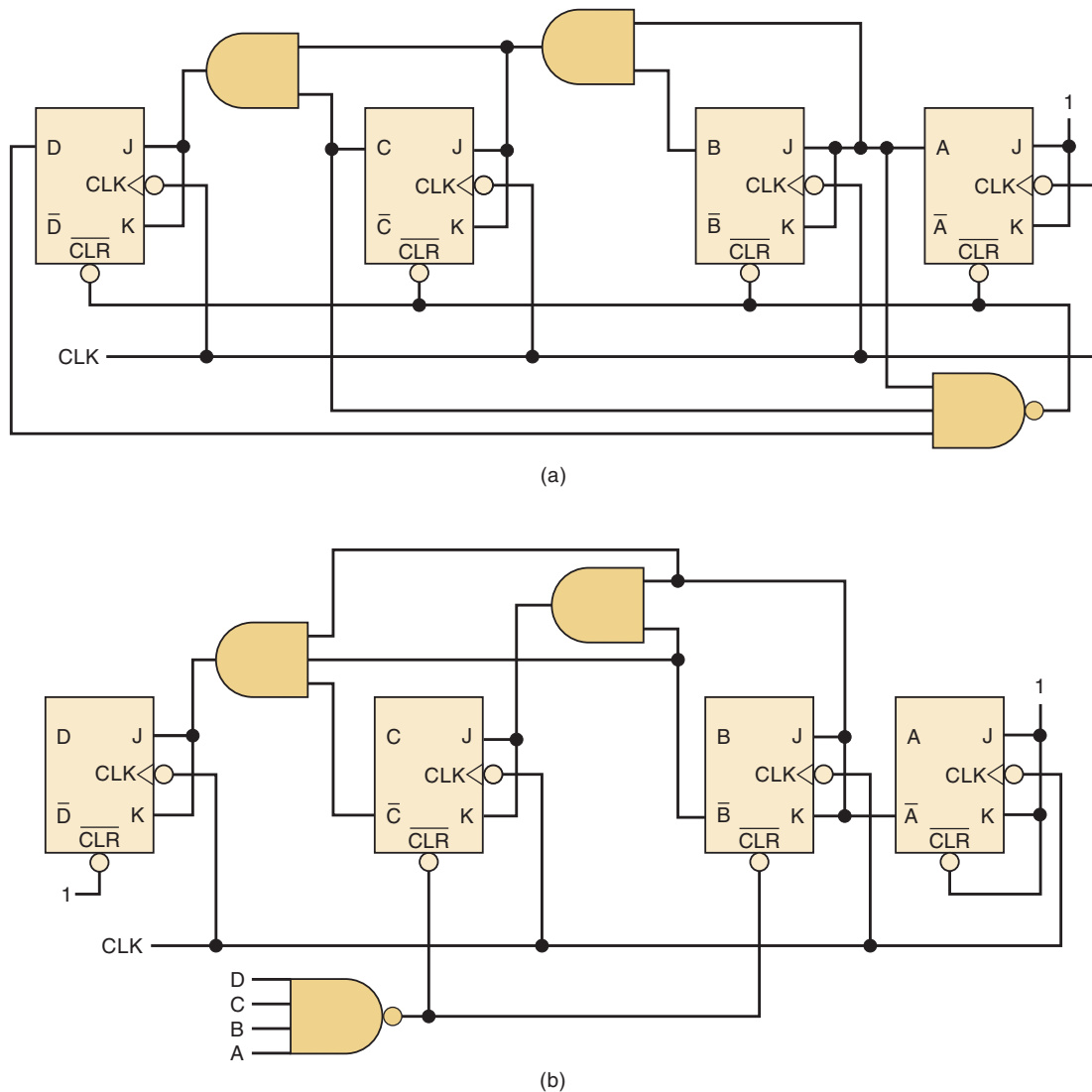


FIGURE 7-110 Problems 7-37 and 7-38.

- C** 7-41* Analyze the synchronous counter in Figure 7-112(a). F is a control input. Draw its state transition diagram and determine the counter's modulus.
- C** 7-42. Analyze the synchronous counter in Figure 7-112(b). Draw its complete state transition diagram and determine the counter's modulus. Is the counter self-correcting?

SECTION 7-10

- D** 7-43*(a) Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 101, 110, and repeat. The undesired (unused) states 001, 011, 100, and 111 must always go to 000 on the next clock pulse.
- (b) Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares. Compare with the design from (a).

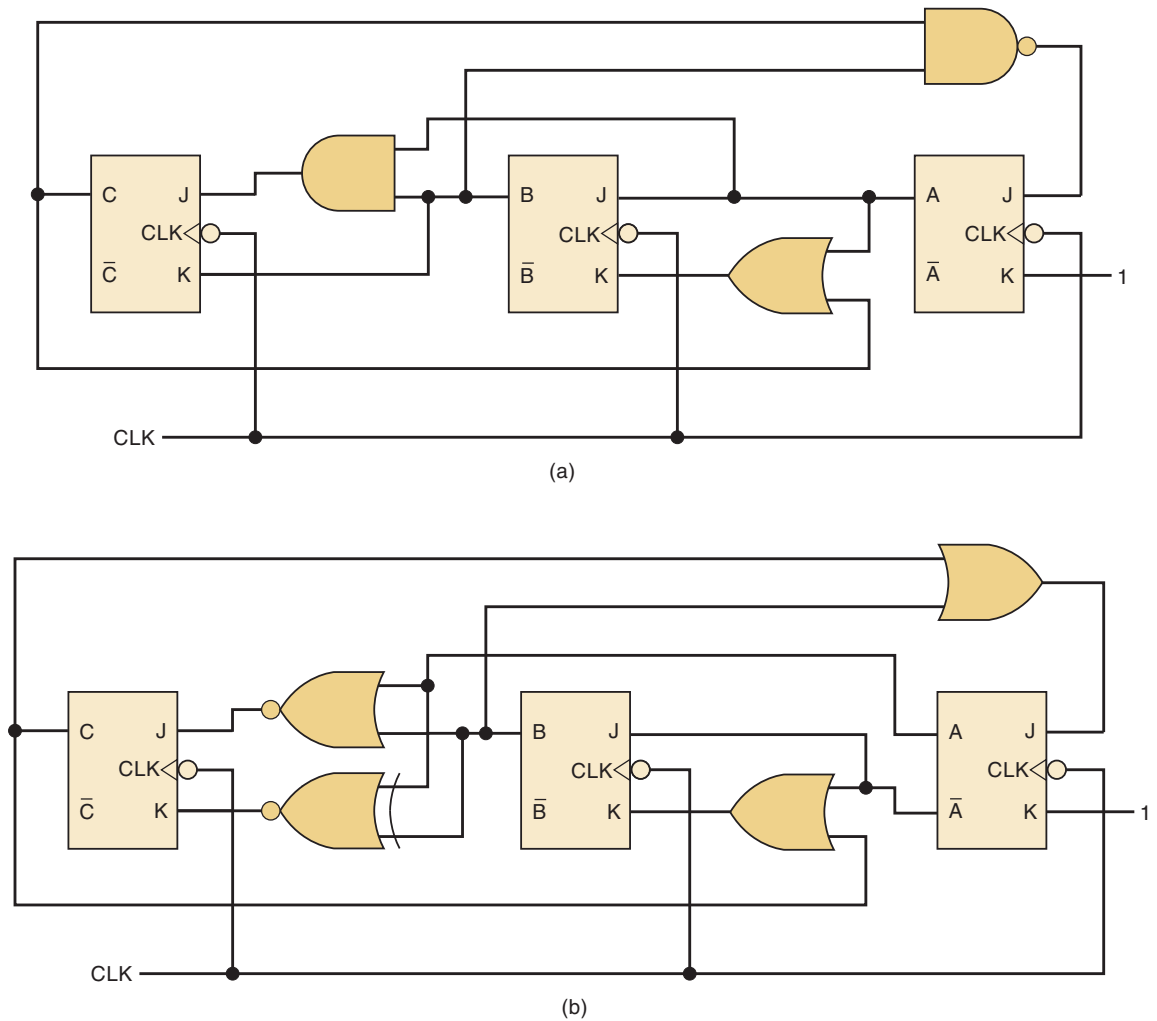
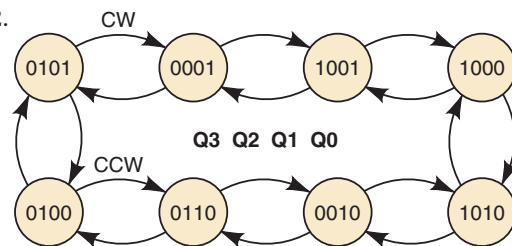


FIGURE 7-111 Problems 7-39 and 7-40.

- D** 7-44. Design a synchronous, recycling, MOD-5 down counter that produces the sequence 100, 011, 010, 001, 000, and repeat. Use J-K flip-flops.
 - (a) Force the unused states to 000 on the next clock pulse.
 - (b) Use don't-care NEXT states for the unused states. Is this design self-correcting?
- D** 7-45* Design a synchronous, recycling, BCD down counter with J-K FFs using don't-care NEXT states.
- D** 7-46. Design a synchronous, recycling, MOD-7 up/down counter with J-K FFs. Use the states 000 through 110 in the counter. Control the count direction with input D ($D = 0$ to count up and $D = 1$ to count down).
- D** 7-47* Design a synchronous, recycling, MOD-8, binary down counter with D flip-flops.
- D** 7-48. Design a synchronous, recycling, MOD-12 counter with D FFs. Use the states 0000 through 1011 in the counter.

- H, D, N** 7-50. Design a recycling, MOD-25, down counter. The count sequence should be 11000 through 00000. Simulate (functional) the counter.
- (a) Use LPM_COUNTER.
- (b) Use an HDL.
- H, D** 7-51* Design a recycling, MOD-16 Gray code counter using an HDL. The counter should have an active-HIGH enable (*cnt*). Simulate the counter.
- H, D** 7-52. Design a bidirectional, half-step controller for a stepper motor using an HDL. The direction control input (*dir*) will produce a clockwise (CW) pattern when HIGH or counterclockwise when LOW. The sequence is given in Figure 7-113. Simulate the sequential circuit.

FIGURE 7-113 Problem 7-52.



- H, D, N** 7-53* Design a frequency divider circuit to output a 100-kHz signal. The input frequency is 5 MHz. Simulate (functional) the counter.
- (a) Use LPM_COUNTER.
- (b) Use an HDL.
- H, D, N** 7-54. Design a frequency divider circuit that will output either of two specified frequency signals. The output frequency is selected by the control input *fselect*. The divider will output a frequency of 5 kHz when *fselect* = 0 or 12 kHz when *fselect* = 1. The input frequency is 60 kHz. Simulate (functional) the counter.
- (a) Use LPM_COUNTER. Hints: Create a down counter that reloads the appropriate value (determined by *fselect*) after the terminal state is reached. You will also need one logic gate.
- (b) Use an HDL.
- H, B** 7-55* Expand the full-featured HDL counter in Section 7-12 to a MOD-256 counter. Simulate the counter.
- H, B** 7-56. Expand the full-featured HDL counter in Section 7-12 to a MOD-1024 counter. Simulate the counter.
- H, D, N** 7-57* Design a recycling, MOD-16, down counter. The counter should have the following controls (from lowest to highest priority): an active-LOW count enable (*en*), an active-HIGH synchronous clear (*clr*), and active-LOW synchronous load (*ld*). Decode the terminal count when enabled by *en*. Simulate (functional) the counter. Be sure to verify the decoder operation.
- (a) Use LPM_COUNTER. Use any necessary logic gates.
- (b) Use an HDL.
- H, D, N** 7-58. Design a recycling, MOD-10, up/down counter. The counter will count up when *up* = 1 and will count down when *up* = 0. The counter should also have the following controls (from lowest to highest

priority); an active-HIGH count enable (*enable*), active-HIGH synchronous load (*load*), and an active-LOW asynchronous clear (*clear*). Decode the terminal count when enabled by *enable*. Simulate (functional) the counter.

- (a) Use LPM_COUNTER. Use any necessary logic gates.
- (b) Use an HDL.

SECTION 7-13

- H** 7-59* Create a MOD-1000 BCD counter by cascading together three of the HDL BCD counter modules (described in Section 7-13). Simulate the counter.
- H** 7-60. Create a MOD-256 binary counter by cascading together two of the full-featured, MOD-16, HDL counter modules (described in Section 7-12). Simulate the counter.
- H, D, N** 7-61* Design a synchronous, MOD-50 BCD counter by cascading a MOD-10 and a MOD-5 counter together. The MOD-50 counter should have an active-HIGH count enable (*enable*) and an active-LOW synchronous clear (*clrn*). Be sure to include the terminal count detection for the one's digit to cascade with the ten's digit. Simulate (functional) the counter.
 - (a) Use LPM_COUNTER. Use any necessary logic gates.
 - (b) Use an HDL.
- H, D, N** 7-62. Design a synchronous, MOD-100, BCD down counter by cascading two MOD-10, down counter modules together. The MOD-100 counter should have a synchronous parallel load (*load*). Simulate (functional) the counter.
 - (a) Use LPM_COUNTER.
 - (b) Use an HDL.

SECTION 7-14

- H** 7-63* Modify the HDL description in Figure 7-60 or Figure 7-61 to add a rinse sequence after the clothes are washed. The new state machine sequence should be *idle* → *wash_fill* → *wash_agitate* → *wash_spin* → *rinse_fill* → *rinse_agitate* → *rinse_spin* → *idle*. Use hot water to wash, and cold water to rinse (add output bits to control two water valves). Simulate the modified HDL design.
- H** 7-64. Simulate the HDL traffic light controller design presented in Section 7-14.

PART 2

SECTIONS 7-15 THROUGH 7-16

- B** 7-65* A set of 74ALS174 registers is connected as shown in Figure 7-114. What type of data transfer is performed with each register? Determine the output of each register when the $\overline{MR}$ is pulsed momentarily LOW and after each of the indicated clock pulses (CP#) in Table 7-10. How many clock pulses must be applied before data that are input on *I5–I0* are available at *Z5–Z0*?

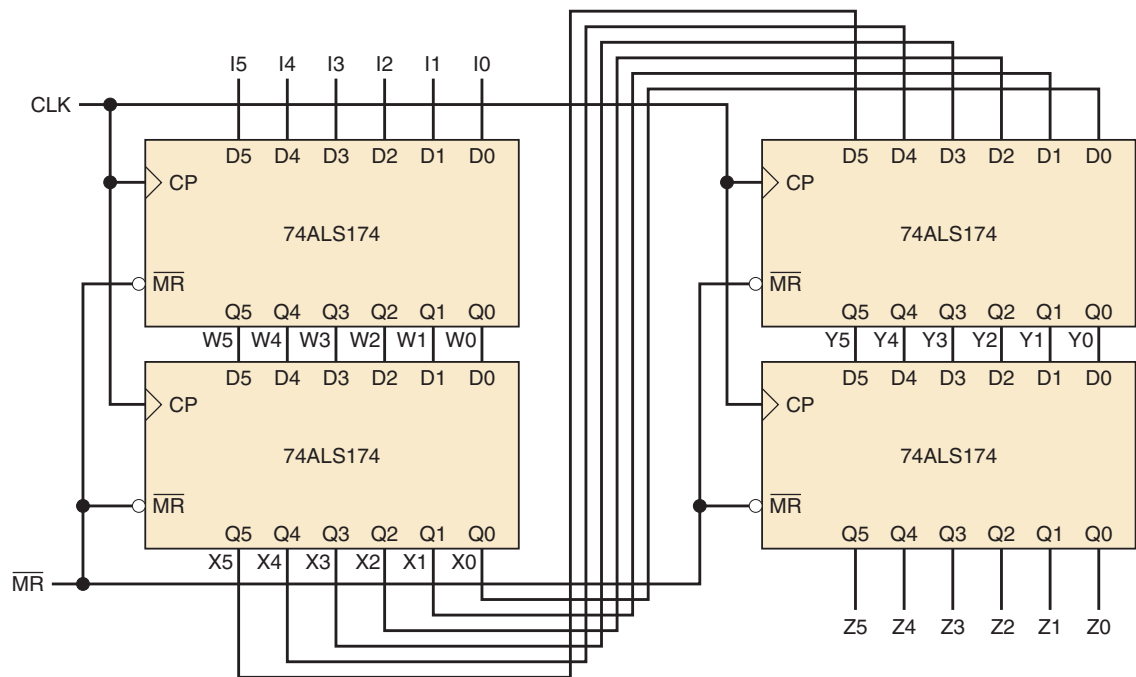


FIGURE 7-114 Problem 7-65.

TABLE 7-10

↑ CLK	$\overline{\text{MR}}$	I5–I0	W5–W0	X5–X0	Y5–Y0	Z5–Z0
X	0	101010				
CP1	1	101010				
CP2	1	010101				
CP3	1	000111				
CP4	1	111000				
CP5	1	011011				
CP6	1	001101				
CP7	1	000000				
CP8	1	000000				

- B** 7-66. Complete the timing diagram in Figure 7-115 for a 74HC174. How does the timing diagram show that the master reset is asynchronous?
- B** 7-67* How many clock pulses will be needed to completely load eight bits of serial data into a 74ALS166? How does this relate to the number of flip-flops contained in the register?
- B** 7-68. Repeat Example 7-20 for the input waveforms given in Figure 7-116.
- 7-69* Repeat Example 7-22 with $D_S = 1$ and the input waveforms given in Figure 7-117.
- 7-70. Apply the input waveforms given in Figure 7-118 to a 74ALS166 and determine the output produced.
- B** 7-71* While examining the schematic for a piece of equipment, a technician or an engineer will often come across an IC that is unfamiliar. In such cases, it is often necessary to consult the manufacturer’s data

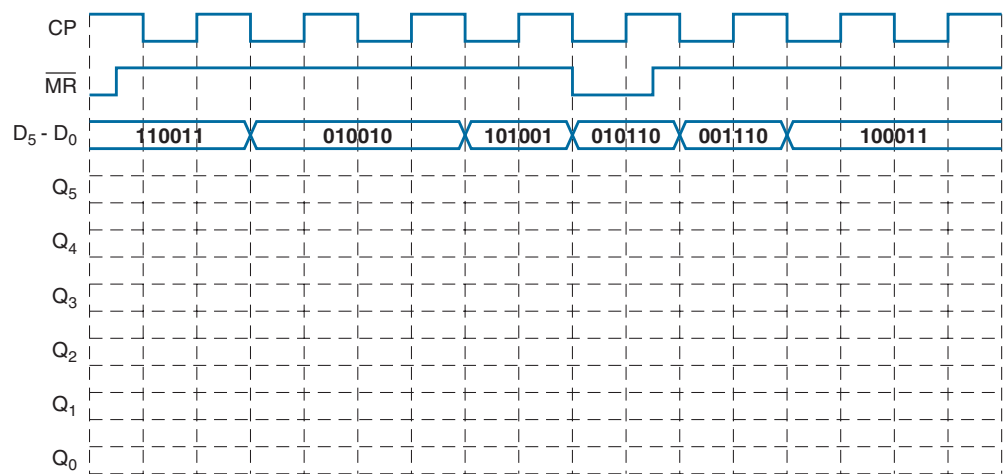


FIGURE 7-115 Problem 7-66.

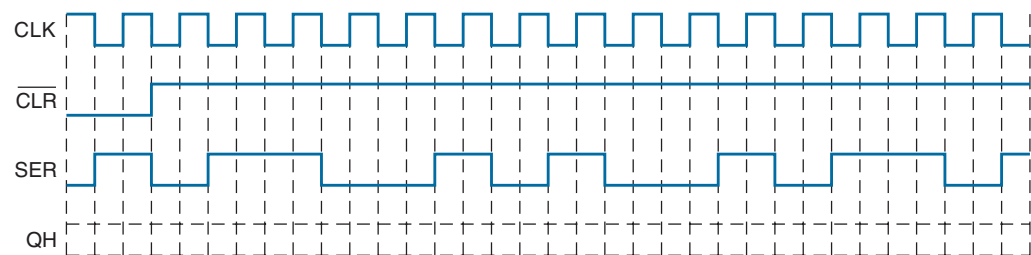


FIGURE 7-116 Problem 7-68.

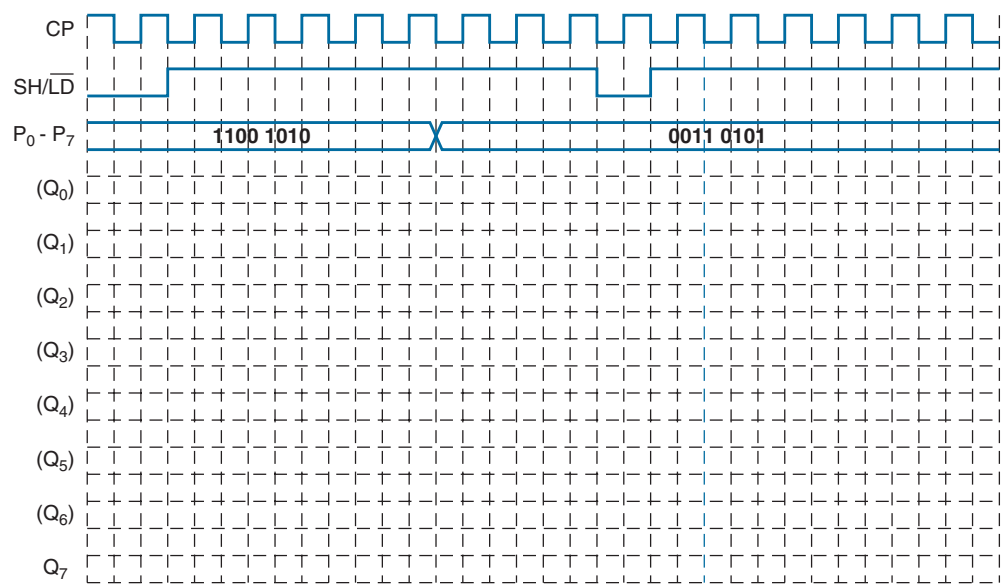
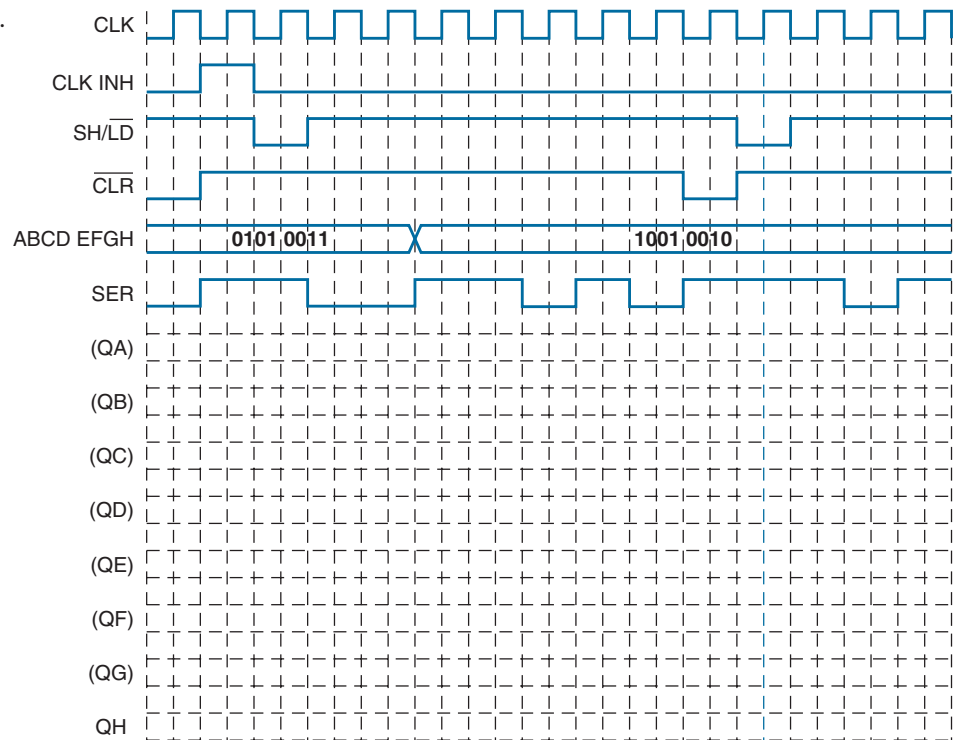


FIGURE 7-117 Problem 7-69.

FIGURE 7-118 Problem 7-70.



sheets for specifications on the device. Research the data sheet for the 74AS194 bidirectional universal shift register to answer the following questions:

- Is the $\overline{CLR}$ input asynchronous or synchronous?
- True or false:* When CLK is LOW, the S_0 and S_1 inputs have no effect on the register.
- Assume the following conditions:

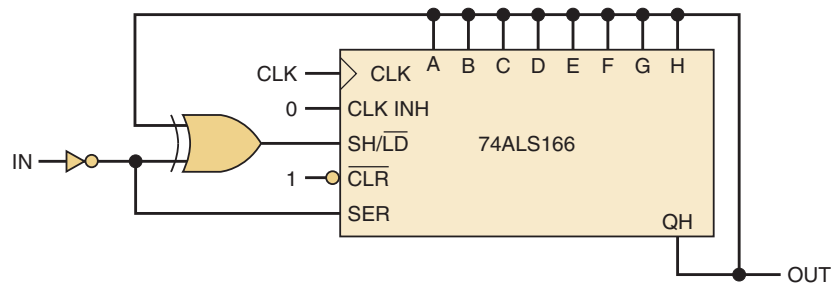
$$\begin{aligned} Q_A \ Q_B \ Q_C \ Q_D &= 1 \ 0 \ 1 \ 1 \\ A \ B \ C \ D &= 0 \ 1 \ 1 \ 0 \\ \overline{CLR} &= 1 \\ SR \ SER &= 0 \\ SL \ SER &= 1 \end{aligned}$$

If $S_0 = 0$ and $S_1 = 1$, determine the register outputs after one CLK pulse. After two CLK pulses. After three. After four.

- Use the same conditions except $S_0 = 1$ and $S_1 = 0$ and repeat part (c).
- Repeat part (c) with $S_0 = 1$ and $S_1 = 1$.
- Repeat part (c) with $S_0 = 0$ and $S_1 = 0$.
- Use the same conditions as in part (c), except assume that Q_A is connected to SL SER . What will be the register outputs after four CLK pulses?

C 7-72. Refer to Figure 7-119 to answer the following questions:

- Which register function (load or shift) will be performed on the next clock if $in = 1$ and $out = 0$? What data value will be input when clocked?

FIGURE 7-119 Problem 7-72.

- Which register function (load or shift) will be performed on the next clock if $in = 0$ and $out = 1$? What data value will be input when clocked?
- Which register function (load or shift) will be performed on the next clock if $in = 0$ and $out = 0$? What data value will be input when clocked?
- Which register function (load or shift) will be performed on the next clock if $in = 1$ and $out = 1$? What data value will be input when clocked?
- What input condition will eventually (after several clock pulses) cause the output to switch states?
- To change the output logic level requires the new input condition to last for at least how many clock pulses?
- If the input signal changes levels and then goes back to its original logic level before the number of clock pulses specified in part (f), what happens to the output signal?
- Explain why this circuit can be used to debounce switches.

SECTION 7-17

- 7-73* Draw the diagram for a MOD-5 ring counter using J-K flip-flops. Make sure that the counter will start the proper count sequence when it is turned on.
- 7-74. Add one more J-K flip-flop to convert the MOD-5 ring counter in Problem 7-73 into a MOD-10 counter. Determine the sequence of states for this counter. This is an example of a decade counter that is not a BCD counter. Draw the decoding circuit for this counter.
- 7-75* Draw the diagram for a MOD-10 Johnson counter using a 74HC164. Make sure that the counter will start the proper count sequence when it is turned on. Determine the count sequence for this counter and draw the decoding circuit needed to decode each of the 10 states. This is another example of a decade counter that is not a BCD counter.
- 7-76. The clock input to the Johnson counter in Problem 7-75 is 10 Hz. What is the frequency and duty cycle for each of the counter outputs?

SECTION 7-18

- 7-77* The MOD-10 counter in Figure 7-8(b) produces the count sequence 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, and repeats. Identify some possible fault conditions that might produce this result.