



EXERCISE 3.4.— Consider the shift register shown in Figure 3.24, which is implemented using D flip-flops and 2 : 1 multiplexers.



Complete the functional truth table shown in Table 3.8.

Inputs			NS			
CK	$\overline{\text{CLR}}$	Load	Q_3^+	Q_2^+	Q_1^+	Q_0^+
x	0	x				
	1	0				
	1	1				

Table 3.8. Functional truth table (NS, next state)

Complete (Q_0 , Q_1 , Q_2 and Q_3) the timing diagram in Figure 3.25 assuming that $X_3X_2X_1X_0 = 0101$.

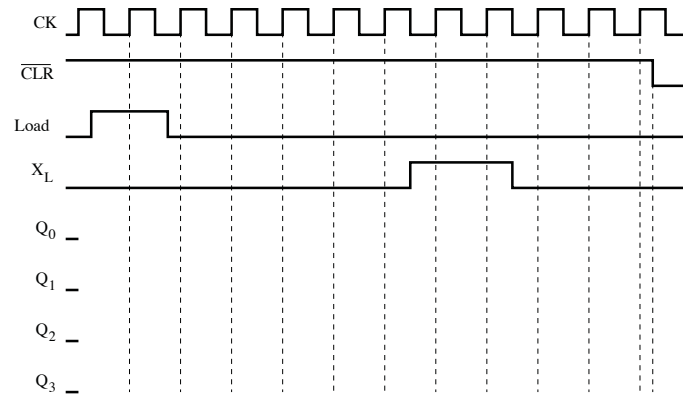


Figure 3.25. Timing diagram ($X_3X_2X_1X_0 = 0101$)

Figure 3.26 depicts the logic circuit for another type of shift register that is also based on D flip-flops and 2 : 1 multiplexers.

Complete the functional truth table represented in Table 3.9.

EXERCISE 3.5.— The universal shift register shown in Figure 3.27 is composed of D flip-flops and 4 : 1 multiplexers. During a normal operation, the synchronous *reset* input is set to 1 and does not affect the outputs.

Complete the functional truth table given in Table 3.10.

Complete the timing diagram shown in Figure 3.28.

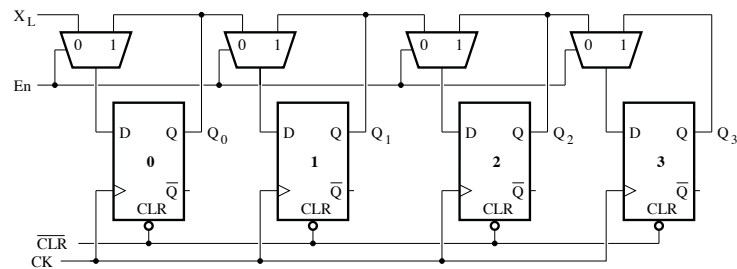


Figure 3.26. Shift register with enable signal

Inputs			NS			
CK	$\overline{\text{CLR}}$	En	Q_3^+	Q_2^+	Q_1^+	Q_0^+
x	0	x				
	1	0				
	1	1				

Table 3.9. Functional truth table (NS, next state)

Inputs				NS			
CK	$\overline{\text{Reset}}$	C_1	C_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+
x	0	x	x				
x	1	0	0				
	1	0	1				
	1	1	0				
	1	1	1				

Table 3.10. Functional truth table

EXERCISE 3.6.– Determine the count sequence for the logic circuit shown in Figure 3.29 assuming that the initial state is $Q_2Q_1Q_0 = 111$, and the count sequence of the circuit shown in Figure 3.30 for a case where the initial state is $Q_2Q_1Q_0 = 000$.

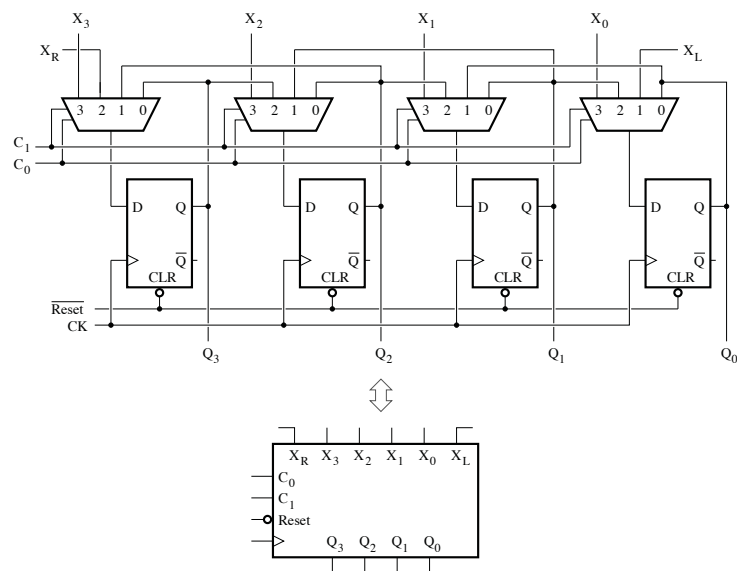


Figure 3.27. Logic circuit and symbol for the four-bit universal shift register

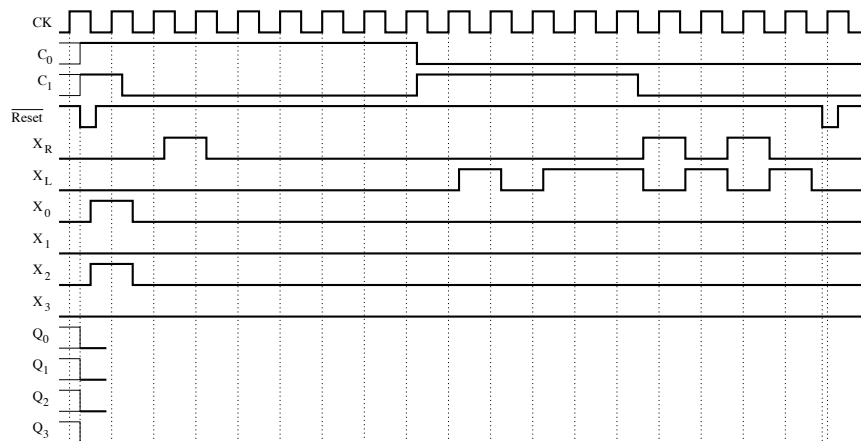


Figure 3.28. Timing diagram for a universal register

EXERCISE 3.7.– Modulo m or $m - 1$ counter.

Consider the counter using two flip-flops shown in Figure 3.31(a).

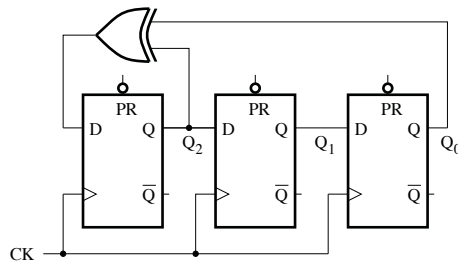


Figure 3.29. Three-bit LFSR counter with flip-flops initially set to 1

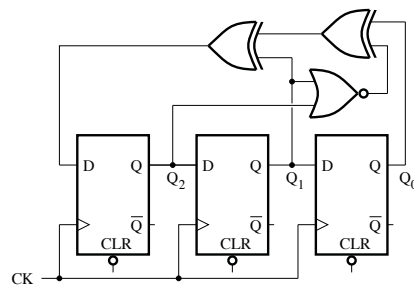


Figure 3.30. Three-bit LFSR counter with flip-flops initially set to 0

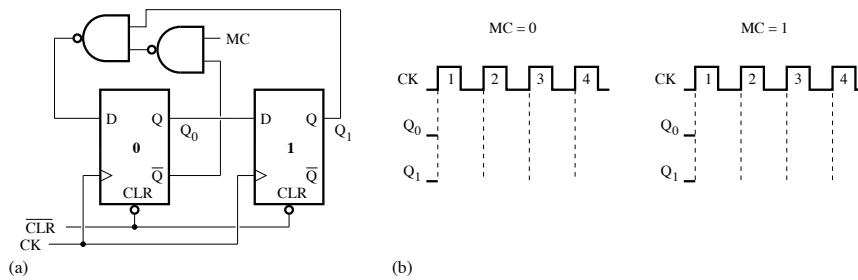


Figure 3.31. Modulo m or $m - 1$ counter with two flip-flops:
a) logic circuit; b) timing diagram

Complete the timing diagrams of Figure 3.31(b) when $MC = 0$ and $MC = 1$. We will assume that the initial state is 0.

Determine the value of the modulo when $MC = 0$ and $MC = 1$.