

EXERCISE 2.4.– Asynchronous circuit using two flip-flops.

The asynchronous circuit shown in Figure 2.24(a) consists of two D flip-flops and a NAND gate.

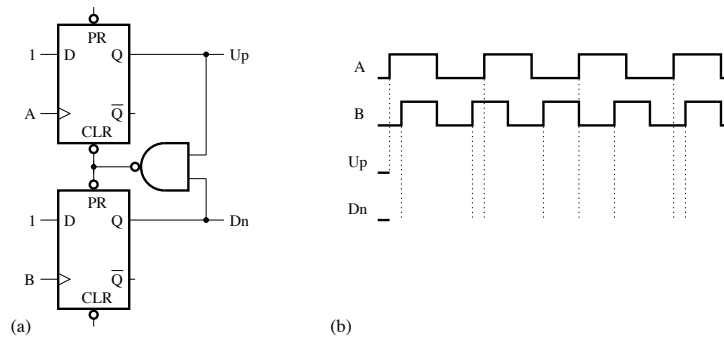


Figure 2.24. a) Asynchronous circuit using two flip-flops;
b) timing diagram

Complete the timing diagram as shown in Figure 2.24(b).

What function does this circuit serve?

EXERCISE 2.5.– Counter using three flip-flops.

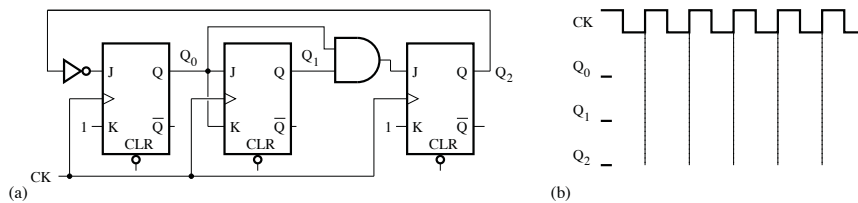


Figure 2.25. a) Counter using three flip-flops; b) timing diagram

Consider the counter shown in Figure 2.25(a), whose flip-flops are initially set to 0:

- determine the logic equations for the J and K inputs of each flip-flop;
- complete the timing diagram in Figure 2.25(b);
- construct the state diagram of the counter;
- deduce the counter modulo.

EXERCISE 2.6.– Counter using four flip-flops.

Give the timing diagram for the counter shown in Figure 2.26, assuming that all the flip-flops are initially set to 0.

Modify the counter shown in Figure 2.26 by adding a set input ($\overline{PR}$) and a reset input ($\overline{CLR}$), which, when activated, determine the state: $Q_3Q_2Q_1Q_0 = 1010$.

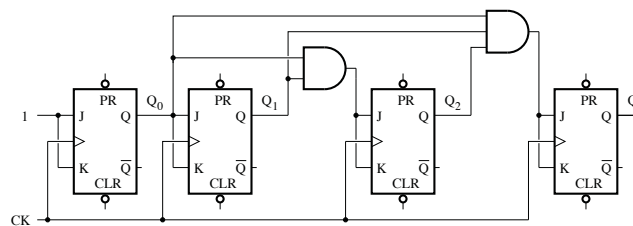


Figure 2.26. Logic circuit for a four-bit counter

EXERCISE 2.7.– Counter using three JK flip-flops.

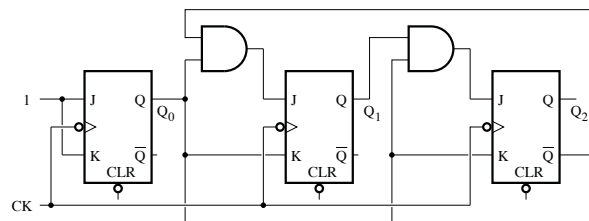


Figure 2.27. Logic circuit for a counter using three JK flip-flops

Consider the logic circuit of the counter shown in Figure 2.27:

- determine the logic equations for the inputs of each flip-flop;
- give the timing diagram for the counter assuming that all the flip-flops are initially reset to 0;
- give the state diagram for the counter;
- deduce the counter modulo.

EXERCISE 2.8.– Synchronous D flip-flop counter.

For the counter shown in Figure 2.28, determine the logic equation of the input for each flip-flop and construct the transition table. We will assume that the initial state of each counter is 0.

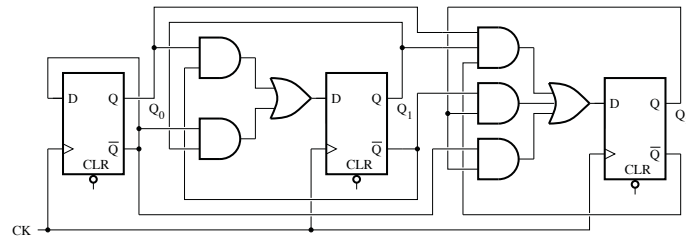


Figure 2.28. Logic circuit for the synchronous D flip-flop counter

Deduce the counter modulo.

EXERCISE 2.9.– The counter shown in Figure 2.29 is initially set to 0 (that is $Q_2Q_1Q_0 = 000$).

- Determine the logic expressions for the inputs J_0 , K_0 , J_1 , K_1 , J_2 and K_2 .
- Derive the state diagram for this counter.

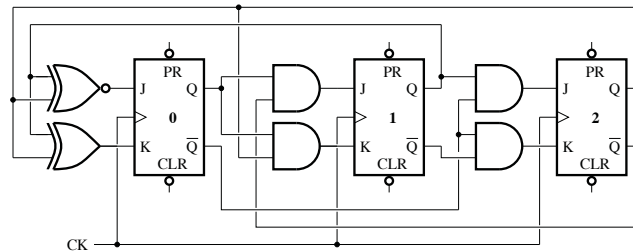


Figure 2.29. Logic circuit for the counter using JK flip-flops

EXERCISE 2.10.– The counter shown in Figure 2.30(a) is initially set to 0 (in other words $Q_2Q_1Q_0 = 001$):

- determine the logic expressions for the inputs J_0 , K_0 , J_1 , K_1 , J_2 and K_2 ;
- complete the timing diagram shown in Figure 2.30(b);
- determine $Q_2 Q_1 Q_0$ when the diode D_7 is switched on;

– can the counter simultaneously switch on both the diodes, D_2 and D_7 ?

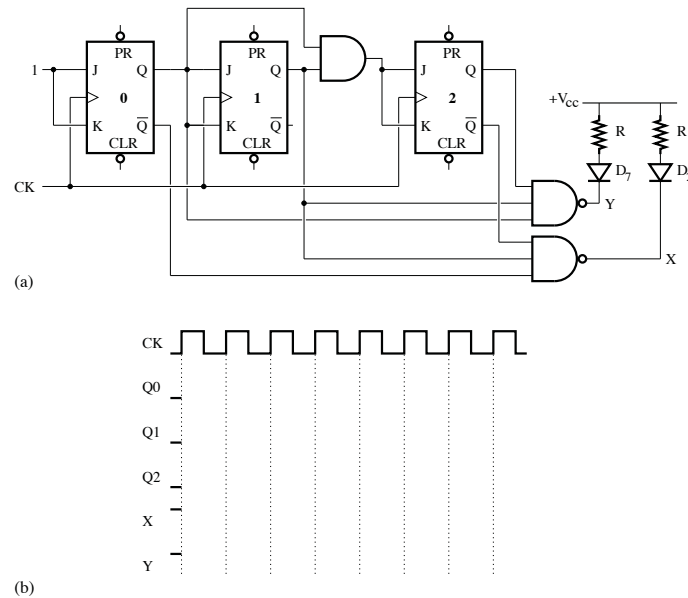


Figure 2.30. a) Counter connected to D_1 and D_2 diodes; b) timing diagram

EXERCISE 2.11.– Synchronous counter.

The synchronous counter shown in Figure 2.31 consists of a debouncing switch (S), a D flip-flop for data synchronization on the falling edge of the clock signal and a counter circuit with a reset push button.

Determine the logic equations for the inputs, D_1 and D_0 , and the outputs, Y_1 and Y_0 , as functions of X , Q_1 and Q_0 .

Complete the timing diagram given in Figure 2.32 and 2.33.

What is the function of the switch S?

Complete the output decoding table given in Table 2.6.

EXERCISE 2.12.– Temporization circuit for a quartz clock.

An m modulo counter can be implemented, as shown in Figure 2.34, with a reset input, $\overline{CLR}$, an enable input, EN , and a ripple-carry output, RCO .

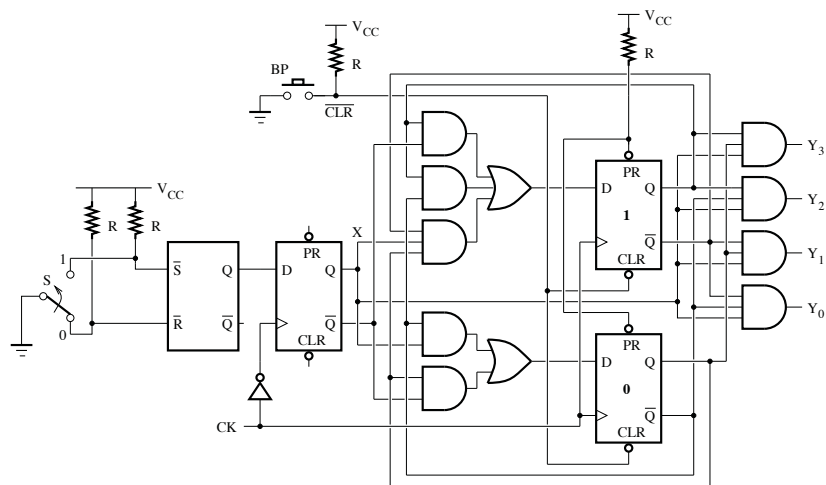


Figure 2.31. Synchronous circuit

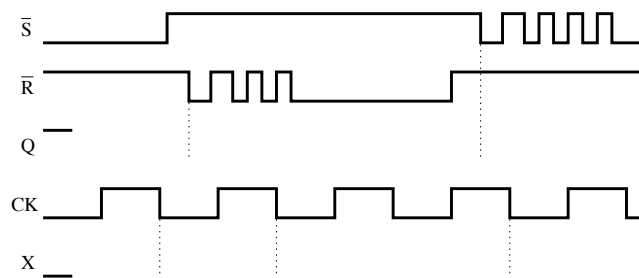


Figure 2.32. Timing diagram 1

X	Q_1	Q_0	Y_3	Y_2	Y_1	Y_0
0	x	x				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

Table 2.6. Output decoding table